

Remarks:

Reconsideration of the application is requested.

Claims 1-14 remain in the application. Claim 10 has been amended.

On August 14, 2002, counsel received a telephone call from the Examiner. The Examiner stated that claims 1-9 were allowable and requested the cancellation of claims 10-14. Counsel declined and now requests the rejoinder of claims 10-14 under MPEP 821.04.

Claim 10 has been amended to include all of the limitations recited in claim 1.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 10. Claim 10 is, therefore, believed to be patentable over the art and since dependent claims 11-14 are ultimately dependent on claim 10, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 10-14 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, he is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



For Applicant

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GR 98 P 2314 P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Siegfried Schwarzl
Applic. No. : 09/781,173
Filed : February 12, 2001
Title : Memory Cell Array And Method For
Manufacturing It
Examiner : Anh K. Phung
Group Art Unit : 2824

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 10 (amended). A method for manufacturing a memory cell
array, which comprises:

applying a first insulating layer to a carrier wafer;

producing a trench having side walls and a bottom in the first
insulating layer;

producing a first yoke that adjoins the side walls of the
trench and that adjoins the bottom of the trench, and
producing the first yoke from a magnetizable material with a
permeability of at least 10;

producing a first line in the trench;

producing a memory element with magnetoresistive effect above the first yoke and connecting the memory element to the first line; [and]

producing a second line above the memory element and connecting the second line to the memory element;

insuring that the memory element is configured at a point of intersection between the first line and the second line;

switching the memory element between the first line and the second line;

configuring the first yoke such that a magnetic flux through the first yoke is essentially closed in the memory element;

during a write access, supplying current to a given line selected from a group consisting of the first line and the second line; and

partially surrounding the given line with the first yoke.